WHAT IS CLAIMED IS:

1. A semiconductor memory element comprising:

a well region having a first conductivity type and formed in a principal surface of a semiconductor substrate;

source and drain regions each having a second conductivity type and formed in said well region to have a specified distance therebetween;

first and second gates and a charge storage region each formed on a portion of the principal surface of said semiconductor substrate interposed between said source and drain regions via a first insulating film; and

a third gate formed over said charge storage region via a second insulating film,

said charge storage region being provided between said first and second gates.

2. A semiconductor memory element comprising:

a well region having a first conductivity type and formed in a principal surface of a semiconductor substrate;

source and drain regions each having a second conductivity type and formed in said well region to have a specified distance therebetween;

first and second gates each formed on a portion of the principal surface of said semiconductor substrate interposed between said source and drain regions via a first insulating film;

a charge storage region formed on said semiconductor substrate via a second insulating film; and

a third gate formed over said charge storage region via a third insulating film,

said charge storage region being provided between said first and second gates.

3. The semiconductor memory element of claim 2, wherein said first insulating film is different in thickness from said second insulating film.

4. A semiconductor memory element comprising:

a well region having a first conductivity type and formed in a principal surface of a semiconductor substrate;

source and drain regions each having a second conductivity type and formed in said well region to have a specified distance therebetween in a first direction;

first and second gates each formed on a portion of the principal surface of said semiconductor substrate interposed between said source and drain regions via a first insulating film;

a charge storage region formed on said semiconductor substrate via a second insulating film; and

a third gate formed over said charge storage region via a third insulating film,

said first and second gates being formed in parallel with said first direction,

said third gate being formed in a direction orthogonal to said first direction,

said charge storage region being provided between said first and second gates.

5. The semiconductor memory element of claim 1, wherein said charge storage region has a layer composed of a plurality of semiconductor nano-crystals.

6. The semiconductor memory element of claim 1, wherein said charge storage region has a silicon nitride thin film.

7. The semiconductor memory element of claim 1, wherein said charge storage region has a silicon oxynitride thin film.

8. The semiconductor memory element of claim 1, wherein said charge storage region has a floating gate composed of polysilicon.

9. The semiconductor memory element of claim 2, wherein said third insulating film is composed of a silicon dioxide doped with nitrogen.

10. A semiconductor memory device having a memory cell array composed of an arrangement of a plurality of the semiconductor memory elements as recited in claim 4, said semiconductor memory device comprising:

first local bit lines each connecting respective drain regions of said plurality of semiconductor memory elements arranged in the first direction;

second local bit lines each connecting respective source regions of said plurality of semiconductor memory elements connected by the corresponding one of said first local bit lines,

first assist gate lines each connecting respective first gates of said plurality of semiconductor memory elements each connected by the corresponding one of said first local bit lines;

second assist gate lines each connecting respective second gates of said plurality of semiconductor memory elements each connected by the corresponding one of said first local bit lines; and

word lines each connecting respective third gates of said plurality of semiconductor memory elements arranged in the direction orthogonal to said first direction,

said plurality of semiconductor memory elements connected by one of said first local bit lines being connected individually to the different word lines.

11. A semiconductor memory device of claim 10, wherein, when information is written in one of said semiconductor memory elements,

0 V is applied to each of the first and second assist gates of the first semiconductor memory element adjacent to said one of the semiconductor memory elements on one side thereof and sharing the corresponding one of said word lines with said one of the semiconductor memory elements and

0 V is applied to each of the first and second assist gates of the second semiconductor memory element adjacent to said one of the semiconductor memory elements on the other side thereof and sharing the word line with said one of the semiconductor memory elements.

12. The semiconductor memory device of claim 10, wherein said first assist gate lines are tied on an every other line basis at one end of said memory array, while said second assist gate lines are tied on an every other line basis at the other end of said memory array.

13. A semiconductor memory element comprising:

a well region having a first conductivity type and formed in a principal surface of a semiconductor substrate;

source and drain regions each having a second conductivity type and formed in said well region to have a specified distance therebetween;

a first gate formed on a portion of the principal surface of said semiconductor substrate interposed between said source and drain regions via a first insulating film;

first and second charge storage regions each formed on said semiconductor substrate via a second insulating film; and

a second gate formed over said first and second charge storage regions via a third insulating film,

said first charge storage region being provided between said first gate and said source region via said second insulating film and said second charge storage region being provided between said first gate and said drain region via said second insulating film.

14. The semiconductor memory element of claim 13, wherein each of said first and second charge storage regions has a layer composed of a plurality of semiconductor nano-crystals.

15. The semiconductor memory element of claim 13, wherein each of said first and second charge storage regions has a silicon nitride thin film.

16. The semiconductor memory element of claim 13, wherein each of said first and second charge storage regions has a silicon oxynitride thin film.

17. The semiconductor memory element of claim 13, wherein each of said first and second charge storage regions has a floating gate composed of polysilicon.

18. The semiconductor memory element of claim 13, wherein said third insulating film is composed of a silicon dioxide doped with nitrogen.

19. A semiconductor memory device having a memory cell array composed of an arrangement of a plurality of the semiconductor memory elements as recited in claim 13, said semiconductor memory device comprising:

first local bit lines each connecting respective drain regions of said plurality of semiconductor memory elements arranged in a first direction;

second local bit lines each connecting respective source regions of said plurality of semiconductor memory elements connected by the corresponding one of said first local bit lines,

assist gate lines each connecting respective first gates of said plurality of semiconductor memory elements each connected by the corresponding one of said first local bit lines; and

word lines each connecting respective third gates of said plurality of semiconductor memory elements arranged in a direction orthogonal to said first direction,

said plurality of semiconductor memory elements connected by one of said first local bit lines being connected individually to the different word lines.

20. A semiconductor memory device of claim 19, wherein, when information is written in one of said semiconductor memory elements,

0 V is applied to the assist gate of the first semiconductor memory element adjacent to said one of the semiconductor memory elements on one side thereof and sharing the corresponding one of said word lines with said one of the semiconductor memory elements and

0 V is applied to the assist gate of the second semiconductor memory element adjacent to said one of the semiconductor memory elements on the other side thereof and sharing the word line with said one of the semiconductor memory elements.

21. The semiconductor memory device of claim 19, wherein said assist gate lines are tied on an every other line basis at one end of said memory array.

22. A semiconductor memory element comprising:

a well region having a first conductivity type and formed in a principal surface of a semiconductor substrate;

source and drain regions each having a second conductivity type and formed in said well region to have a specified distance therebetween;

a first gate formed on a portion of the principal surface of said semiconductor substrate interposed between

said source and drain regions via a first insulating film; and

first and second charge storage regions each formed on said semiconductor substrate via a second insulating film;

a second gate formed over said first charge storage region via a third insulating film; and

a third gate formed over said second charge storage region via the third insulating film,

said first gate being formed in a direction orthogonal to said first direction,

each of said second and third gates being formed in parallel with said first direction,

said first charge storage region being provided between said first gate and said source region via said second insulating film and said second charge storage region being provided between said first gate and said drain region via said second insulating film.

23. The semiconductor memory element of claim 22, wherein each of said first and second charge storage regions has a layer composed of a plurality of semiconductor nano-crystals.

24. The semiconductor memory element of claim 22, wherein each of said first and second charge storage regions has a silicon nitride thin film.

25. The semiconductor memory element of claim 22, wherein each of said first and second charge storage regions has a silicon oxynitride thin film.

26. The semiconductor memory element of claim 22, wherein each of said first and second charge storage regions has a floating gate composed of polysilicon.

27. The semiconductor memory element of claim 22, wherein said third insulating film is composed of a silicon dioxide doped with nitrogen.

28. A semiconductor memory device having a memory cell array composed of an arrangement of a plurality of the semiconductor memory elements as recited in claim 22, said semiconductor memory device comprising:

first local bit lines each connecting respective drain regions of said plurality of semiconductor memory elements arranged in the first direction;

second local bit lines each connecting respective source regions of said plurality of semiconductor memory elements connected by the corresponding one of said first local bit lines,

assist gate lines each being connecting respective first gates of said plurality of semiconductor memory elements each connected by the corresponding one of said first local bit lines; and

word lines each connecting respective third gates of said plurality of semiconductor memory elements arranged in the direction orthogonal to said first direction,

said plurality of semiconductor memory elements connected by one of said first local bit lines being connected individually to the different word lines.

29. A semiconductor memory device of claim 28, wherein, when information is written in one of said semiconductor memory elements,

0 V is applied to the assist gate of the first semiconductor memory element adjacent to said one of the semiconductor memory elements on one side thereof and sharing the corresponding one of said word lines with said one of the semiconductor memory elements and

0 V is applied to the assist gate of the second semiconductor memory element adjacent to said one of the semiconductor memory elements on the other side thereof and sharing the word line with said one of the semiconductor memory elements.

30. The semiconductor memory device of claim 28, wherein said assist gate lines are tied on an every fourth line basis at an end of said memory array.